AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a first output terminal, and a scan output terminal, said test circuit comprising:

~~plural~~ a plurality of flip-flops, ~~of a scanning type (FFs, hereinafter)~~ each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input terminal of one of said plurality of serially connected flip-flops, so as to measure an alternating current ~~(AC, hereinafter)~~ characteristic of ~~an~~ the input terminal or the first output terminal of said logical integrated circuit,

wherein said scan path connects ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at an end of ~~said~~ the first stage with ~~a~~ the scan output terminal of said logical integrated circuit.

2. (Currently amended) A test circuit for a logical integrated circuit having a first input terminal, an output terminal, and a scan input terminal, said test circuit comprising:

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n-th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input terminal of one of said plurality of serially connected flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the first input terminal or the output terminal of said logical integrated circuit,

wherein said scan path connects ~~a~~ the scan input terminal of said logical integrated circuit with ~~an~~ the input terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said n-th~~ the nth stage.

3. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a first output terminal, and a scan output terminal, said test circuit comprising:

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n-th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input of one of said plurality of serially connected flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the input terminal or the first output terminal of said logical integrated ~~circuits~~ circuit, wherein:

~~wherein~~ said scan path connects ~~a~~ the scan input with ~~an~~ the input terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said n th~~ the nth stage,

~~again successively~~ from the output of the flip-flop located at the end of the nth stage, said scan path further connects ~~said FFs arranged~~ the flip-flops in ~~said~~ the second to ~~(n-1) th~~ the (n-1)th stages in series, ~~after restarting from an output terminal of said FF standing at an end of said n th stage,~~

~~once again~~ said scan path then connects ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said (n-1) th~~ the (n-1)th stage with ~~an~~ the input terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said~~ the first stage, and

the scan path finally connects ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said~~ the first stage with ~~a~~ the scan output terminal of said logical integrated circuit.

4. (Currently amended) A method ~~for~~ of testing a logical integrated circuit, ~~which is compose of:~~ the logical integrated circuit comprising:

an input terminal,

a first output terminal,

a scan output terminal,

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input of one of said plurality of serially connected flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the input terminal or the first output terminal of said logical integrated circuit, said method comprising: ~~the steps of:~~

connecting ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said~~ the first stage with ~~a~~ the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to ~~one of said~~ the input ~~terminals~~ terminal of said logical integrated circuit, and

measuring ~~said AC~~ the alternating current characteristic of ~~said one of said~~ the input ~~terminals~~ terminal of said logical integrated circuit by inspecting ~~an~~ the output of ~~said~~ the scan output terminal of said logical integrated circuit.

5. (Currently amended) A method ~~for~~ of testing a logical integrated circuit, ~~which is composed of:~~ the logical integrated circuit comprising:

a first input terminal,

an output terminal,

a scan input terminal,

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n-th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input of one of said plurality of serially connected flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the first input terminal or the output terminal of said logical integrated circuit, said method comprising: ~~the steps of:~~

connecting ~~a~~ the scan input terminal of said logical integrated circuit with ~~an~~ the input

terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said n-th~~ the nth stage,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to ~~a~~ the scan input terminal of said logical integrated circuit, and

measuring ~~an AC~~ the alternating current characteristic of ~~one of said~~ the output ~~terminals~~ terminal of said logical integrated circuit by inspecting ~~an~~ the output of ~~said one of said~~ the output ~~terminals~~ terminal of said logical integrated circuit.

6. (Currently amended) A method ~~for~~ of testing a logical integrated circuit, ~~which is composed of:~~ the logical integrated circuit comprising:

a first input terminal

a first output terminal,

a scan input terminal,

a scan output terminal,

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n-th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops

through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input of one of said plurality of serially connected flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the first input terminal or the first output terminal of said logical integrated circuit, said method comprising: ~~the steps of:~~

connecting ~~a~~ the scan input terminal of said logical integrated circuit with ~~an~~ the input terminal of ~~said FF standing a~~ the flip-flop located at the head of ~~said n th~~ the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

connecting ~~said FFs arranged in said~~ the flip-flops in the second to ~~(n-1) th~~ the (n-1)th stages ~~successively~~ in series, ~~after restarting from an output terminal of said FF standing at an end of said n th stage,~~

connecting ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said (n-1) th~~ the (n-1)th stage with ~~an~~ the input terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said~~ the first stage,

connecting ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said~~ the first stage with ~~a~~ the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a scan input signal to the scan input terminal of said logical integrated circuit,

inputting a predetermined data signal to ~~one of said~~ the first input ~~terminals~~ terminal of said logical integrated circuit, and

measuring ~~said AC~~ the alternating current characteristic of ~~said one of said~~ the first

input ~~terminals~~ terminal of said logical integrated circuit by inspecting an output of ~~said~~ the scan output terminal of said logical integrated circuit.

7. (Currently amended) A method ~~for~~ of testing a logical integrated circuit, ~~which is composed of:~~ the logical integrated circuit comprising:

a first input terminal

a first output terminal,

a scan input terminal,

a scan output terminal,

~~plural~~ a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in ~~first to n th~~ a matrix having n stages, ~~in each of which said FFs are successively~~ each stage comprising m flip-flops connected in series,

~~plural~~ a like plurality of logic gates, each logic gate having an output ~~terminals of which are respectively~~ terminal connected ~~with~~ to an input ~~terminals~~ terminal of a respective one of said ~~plural FFs~~ plurality of flip-flops, and

means forming a scan path ~~which is formed of a series connection of a part or a whole~~ serially connecting at least some of said ~~plural FFs, and propagates~~ plurality of flip-flops through the respective logic gates, to propagate a test pattern ~~for measuring~~ applied to the input of one of said plurality of flip-flops, so as to measure an ~~AC~~ alternating current characteristic of ~~an~~ the first input terminal or the first output terminal of said logical integrated circuit, said method comprising: ~~the steps of:~~

connecting ~~a~~ the scan input terminal of said logical integrated circuit with ~~an~~ the input

terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said n th~~ the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

connecting ~~said FFs arranged in said~~ the flip-flops in the second to ~~(n-1) th~~ the (n-1)th stages ~~successively~~ in series, ~~after restarting from an output terminal of said FF standing at an end of said n th stage,~~

connecting ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said (n-1) th~~ the (n-1)th stage with ~~an~~ the input terminal of ~~said FF standing~~ the flip-flop located at ~~a~~ the head of ~~said~~ the first stage,

connecting ~~an~~ the output terminal of ~~said FF standing~~ the flip-flop located at ~~an~~ the end of ~~said~~ the first stage with ~~a~~ the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to ~~a~~ the scan input terminal of said logical integrated circuit, and

measuring ~~an AC~~ the alternating current characteristic of ~~one of said~~ the first output ~~terminals~~ terminal of said logical integrated circuit by inspecting ~~an~~ the output of ~~said~~ the ~~one of said~~ output ~~terminals~~ terminal of said logical integrated circuit.

8. (New) A test circuit for a logical integrated circuit having an input terminal, a first output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops

connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the input terminal or the first output terminal of said logical integrated circuit,

wherein said scan path connects the output terminal of the flip-flop located at an end of the first stage with the scan output terminal of said logical integrated circuit.

9. (New) A test circuit for a logical integrated circuit having a first input terminal, an output terminal, and a scan input terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the first input terminal or the output terminal of said logical integrated circuit,

wherein said scan path connects the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage.

10. (New) A test circuit for a logical integrated circuit having an input terminal, a

first output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the input terminal or the first output terminal of said logical integrated circuit, wherein:

said scan path connects the scan input with the input terminal of the flip-flop located at the head of the nth stage,

from the output of the flip-flop located at the end of the nth stage, said scan path further connects the flip-flops in the second to the (n-1)th stages in series,

said scan path then connects the output terminal of the flip-flop located at the end of the

(n-1)th stage with the input terminal of the flip-flop located at the head of the first stage, and

the scan path finally connects the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit.

11. (New) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

an input terminal,

a first output terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the input terminal or the first output terminal of said logical integrated circuit, said method comprising:

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the input terminal of said logical integrated circuit by inspecting the output of the scan output terminal of said logical integrated circuit.

12. (New) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a first input terminal,

an output terminal,

a scan input terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the first input terminal or the output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.

13. (New) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a first input terminal

a first output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input of one of said plurality of serially connected flip-flops, so as to measure an alternating current characteristic of the first input terminal or the first output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

connecting the flip-flops in the second to the (n-1)th stages in series,

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a scan input signal to the scan input terminal of said logical integrated circuit,

inputting a predetermined data signal to the first input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the first input terminal of said

logical integrated circuit by inspecting an output of the scan output terminal of said logical integrated circuit.

14. (New) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a first input terminal

a first output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path serially connecting at least some of said plurality of flip-flops, to propagate a test pattern applied to the input of one of said plurality of flip-flops, so as to measure an alternating current characteristic of the first input terminal or the first output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

connecting the flip-flops in the second to the (n-1)th stages in series,

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage

with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the first output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.